A Fully Monolithic HMIC Low Noise Amplifier

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Abstract
A two/three stage monolithic silicon low noise amplifier has been designed utilizing SPICE modeling techniques. The circuit design architecture is based on high frequency, small signal BJT's, consisting of an grounded emitter stage at the input and a Darlington configured pair at the device output. A resistor network, with a bypass capacitor, is utilized not only to provide proper DC biasing for each stage, but also obtain impedance matching to 50 ohms at the circuit input and output and to provide RF feedback for the desired broad band gain response.

A patented HMIC glass process is employed to provide both the required collector isolation between active device stages and as an extremely low loss dielectric medium for minimum parasitic, high Q passive, reactive elements.

Introduction
The design and manufacture of silicon based integrated circuits, except in the most simple circuit configurations, requires that the active devices have all three terminals capable of being electrically isolated. This is true for both low frequency linear integrated circuits and operational amplifiers, and for multi-gigahertz high frequency structures. This isolation is normally achieved by utilizing P-type silicon substrates on which a variety of N/N+ silicon epitaxial layers are deposited. Lateral isolation between devices is then achieved by either, in the case of low frequency devices, a deep P-type guard ring diffusion surrounding each of the active devices through the N/N+ films into the P-type substrate; or, for RF frequency circuit structures, via vertical trenching with a dielectric backfill, again surrounding each active device and through the N/N+ epitaxial layer into the underlying P-type region.

In the realization of the amplifier presented in this paper, a new and radically different isolation technology, the Heterolithic Microwave Integrated Circuit, is employed. In this technology, two different materials, glass and silicon - thus, the term *hetero*, are joined into a single monolithic structure.

Discussion
In the design of RF frequency silicon integrated circuits, the limitation in overall circuit performance is generally not the frequency response of the active elements, but more typically the loss of the passive reactive elements, inductors and capacitors, is by far the constraining factor in the high frequency functionality. This can seen in the design topology of representative silicon MMIC's, where the most common matching element is either a resistor or another active device, rarely includes a capacitor, and essentially never includes inductors.

The reason that capacitors and inductors have been avoided in the design and manufacture of silicon high frequency integrated circuits relates to the fact that there is no equivalent to the insulating substrate as is found in Gallium Arsinide and other III-V compound semiconductors. This lack of an insulating substrate then requires that the passivating dielectric which covers the surface of silicon integrated circuits be employed as the insulative film onto which the reactive components are constructed. Since this passivating dielectric is relatively thin, capacitors and especially inductors will be highly coupled to the underlying lossy silicon. The extent of this problem is emphasized by recent articles where spiral inductors having a Q, the ratio of the reactance to the resistance of the element, of 12 were reported as being representative of the state-of-the-art for silicon based MMIC's.

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Initially, HMIC was developed as a glass realization and replacement for ceramic or teflon/fiberglass based microwave integrated circuits. In this HMIC format, all high frequency transmission lines and coupling structures, all inductive and capacitive passive elements, all resistive elements, and all front-to-back electrical and thermal vias would be monolithically achieved utilizing semiconductor based wafer fabrication techniques. In terms of the ability of this technology to produce low loss reactive elements, inductors having a Q as high as 50 and capacitors with a Q of geater than 100 at 2.0 GHz are routinely fabricated. When viewed as an integration technology HMIC can be conceived to produce resistive and reactive passive elements which encompass small size, low cost, and low loss for high performance microwave integrated circuits; furthermore, design and

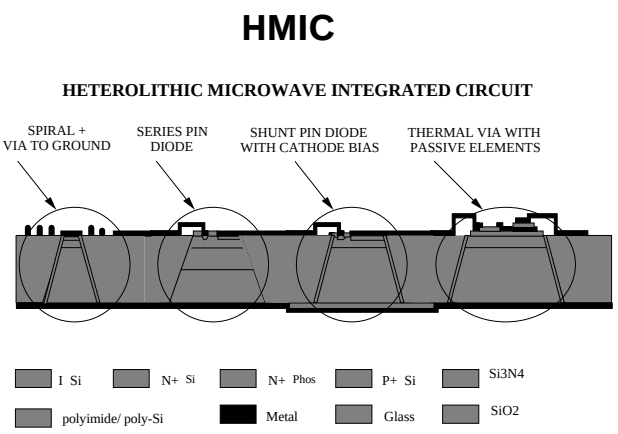

Figure 1 - Crossection of HMIC Structure

process development has quickly led to the incorporation of isolated, active high frequency device structures.

In Figure 1, a generalized crossection for both passive and active based HMIC is presented. This side view is a diagrammatical representation of all the elements required for the construction of any passive or active HMIC circuit fully embedded in low loss glass.

As can be seen HMIC circuits are three dimensional structures. Silicon vias to achieve vertical connections, i.e. front to back, are a natural consequence of the HMIC fabrication process. The top surface of these vias typically serves as the "active" layer for the formation of the required electrical devices and passive elements. The various circuit elements are then laterally interconnected using standard metallization and photolithographic techniques. In addition, as shown in this crossection, electrical structures can even be defined on the back of the HMIC die which allows more circuit complexity to be achieved in a significantly smaller area. Finally, the same metal-lization and photolithographic techniques that are used to pattern the frontside of the circuit can be employed on the back. This enables true surface mount circuits to be obtained.

One of the fundamental building blocks in the world of high frequency transceivers is the need for signal amplification in both the receive and transmit modes. To simplify the task of incorporating RF gain into a monolithic HMIC structure, a small signal, low noise approach was chosen. By taking this path, the constraints imposed by the thermal properties of the transistors and the on-chip RF circuitry are greatly reduced. The following describes the design, modeling, and process development of the monolithic HMIC low noise amplifier which was elected as the technology test vehicle.

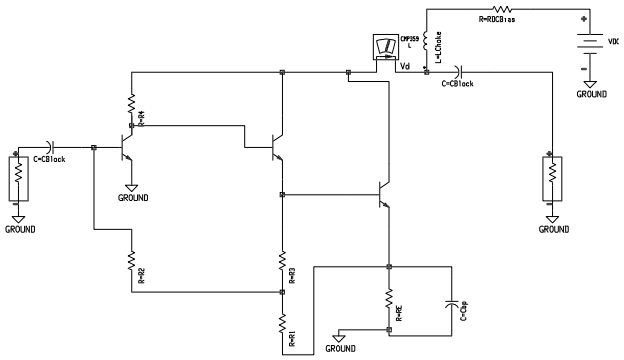

Figure 2 - Monolithic LNA Circuit Schematic

An electrical schematic of the monolithic HMIC low noise amplifier is shown in Figure 2. As can be seen, this design consists of a common emitter first stage which is driving a Darlington pair of devices at the circuit output. An on-chip resistor network, with a high Q, low parasitic monolithic Metal/Nitride/Metal peaking capacitor is utilized in parallel with the emitter feedback resistor located at the circuit output, supplies not only all DC biasing to each gain stage, including a low voltage/low current bias point for the low noise front end, but also provides RF feedback in order to control the gain versus frequency response of the amplifier. Converting the electrical schematic into a

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"SPICE" format enables the RF response of the two stage circuit to be determined. This is presented in Figure 3.

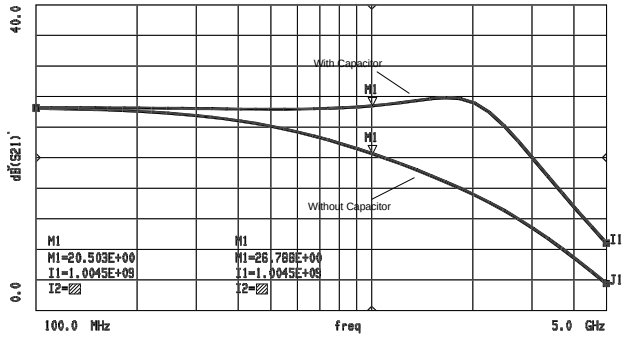

Figure 3 - RF Gain Response With and Without Peaking Capacitor

Figure 3 demonstrates that this monolithic capacitive bypass serves to peak the high end response, while enabling the low frequency gain to remain essentially unaffected. This peaking of gain is quite dramatic; resulting in an approximate 7.0 dB increase in gain at 1.0 GHz; and enabling a significant improvement in the operating bandwidth of the amplifier.

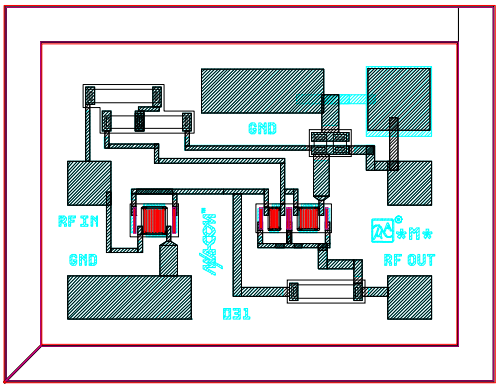

Figure 4 - MDS Layout For HMIC LNA

The RF SPICE simulation of this low noise amplifier circuit predicts 26.8 dB of gain from 100 MHz to approximately 2.3 GHz with a gain flatness of ±0.5 dB. It can also be seen that the simulated 3 dB bandwidth is approximately 3.0 GHz.. Also, as can be seen in Figure 3, SPICE can be used as a very effective equivalent circuit modeling tool to simulate amplifier performance. However, in order to obtain accurate circuit simulations, a reasonable model for the transistors is required. For this amplifier development, silicon BJT's similar to devices produced as discrete products which have an f_t > 10.0 GHz have been employed. As part of the discrete product development, SPICE models were developed as a predictive tool to improve device performance and service the needs of the marketplace. By scaling these existing transistor models, based upon emitter periphery and base area, a more exact fit for the devices employed in the actual HMIC amplifier was obtained.

The use of HMIC glass technology was critical to the design of this amplifier. As can be seen in the circuit schematic shown in Figure 2, it is absolutely necessary from an electrical viewpoint that the collector region of the input stage be both DC and RF isolated from the collectors of the Darlington pair which form the output stage. As can be seen in Figure 4, which is an MDS layout plot of the LNA, this is accomplished by separating the input transistor and the output devices onto separate islands of silicon. A moat region is

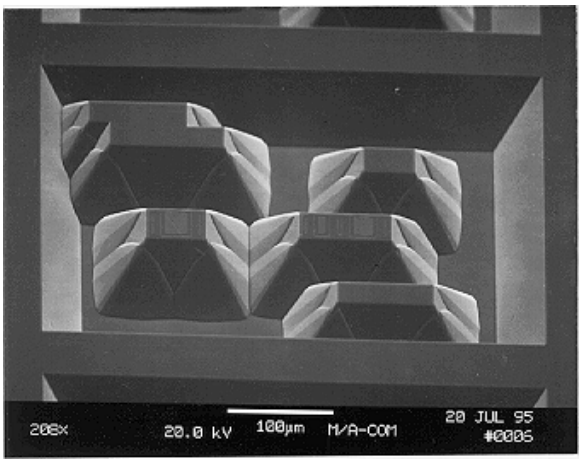

Figure 5 - SEM Photograph of HMIC Island Isolation

formed surrounding these islands by anisotropically etching <1-0-0> silicon, see Figure 5. Glass is then used to fill the moat and provide low loss, low parasitic isolation between circuit stages. The resistive and capacitive feedback and biasing elements are included on the islands adjacent to the transistor structures and utilize the HMIC glass to minimize parasitic reactances. The addition of the appropriate bond pads completes the amplifier physical layout and is completely contained within a die size of 0.40 mm x 0.53 mm.

In Figure 6, a comparison of simulated versus measured RF power gain as a function of frequency is presented for the final HMIC Low Noise Amplifier. It can be seen that the measured performance closely replicates the simulated results up to approximately 1.5 GHz. Above this frequency it can be seen that the gain roll-off occurs sooner than the SPICE simulation

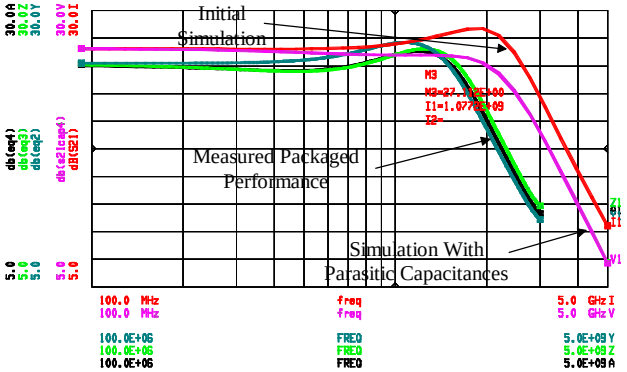

Figure 6 - Measured Versus Simulated Performance

predicts but this is believed to be due to the parasitic reactances associated with the package used for RF measurement of the final circuits.

Conclusions

The present state-of-the-art performance for silicon based MMIC's probably does not appear much different than the predicted performance presented above. However, a common feature that is routinely observed on essentially all commercial silicon MMIC's, is the lack of low loss reactive elements especially inductors. Even the capacitors that are employed are limited to relatively low values, a few picofarads, and typically very lossy due to the MOS construction.

The design and development of this monolithic HMIC low noise amplifier is just the first step in opening a new technology path for silicon based integrated circuits. Now that active devices with gain, in this case high frequency silicon BJT's, have been monolithically embedded into HMIC; which has already demonstrated the ability to incorporate low loss, high Q reactive elements, especially inductors and large value capacitors into high frequency circuits; the functions that can be addressed by silicon MMIC's will be greatly expanded far beyond those currently available in the microwave marketplace. Examples of the high frequency circuits that can be monolithically realized in silicon are VCO's, active mixers, AGC amplifiers, up/down converters, and medium/high power amplifiers. As SiGe HBT's having an $f_t > 40$ GHz become available as a design component, this monolithic HMIC approach should be able to be extended to much higher frequencies.